IN THE CLAIMS

1. (Canceled).

2. (Canceled).

3. (Previously Presented) In an integrated circuit having a system clock, a transmitter comprising:

a transfer clock generator, responsive to the system clock, generating a transfer clock at a high rate relative to the system clock; and

a parallel to serial register, for dividing an input word into a plurality of smaller words and transmitting them over corresponding serial sub-links in response to the transfer clock;

wherein the transfer clock generator comprises a phase locked loop; and

wherein the transmitter is initialized by sending one or more bit alignment code words.

4. (Original) The transmitter as recited in claim 3, wherein a CRC code word is transmitted at intervals.

5. (Canceled).

6. (Canceled).

7. In an integrated circuit having a system clock, a receiver comprising:

a plurality of serial to parallel registers coupled to corresponding serial sub-links, for converting received serial data words from the sub-links into parallel form; and

a clock generator, responsive to the received data, for generating a low speed clock with a frequency nominally equal to the system clock;

a buffer memory in each sub-link for storing a predetermined number of received words; and

a circuit for reading the buffer memories in synchronism under control of the system clock in order to reconstitute the input data word.

8. (Previously Presented) The receiver according to claim 7, wherein the buffer memories each comprise a FIFO register.

9. (Previously Presented) The receiver according to claim 8, wherein the FIFO registers are addressed by an addressing scheme wherein only one bit of the address changes for incremental addresses.

10. (Previously Presented) The receiver according to claim 9, wherein a predetermined bit of the address of each FIFO are compared and employed to generate a trigger signal for actuating a state machine to cause reading of the FIFO registers.

11. (Previously Presented) In an integrated circuit having a system clock, a receiver comprising:

a plurality of serial to parallel registers coupled to corresponding serial sub-links, for converting received serial data words from the sub-links into parallel form; and

a clock generator, responsive to the received data, for generating a low speed clock with a frequency nominally equal to the system clock;

wherein the low speed clock generator includes an edge detector for detecting incoming data and providing an output to a divider for aligning the low speed clock with recovered data and for applying the same to the serial to parallel register for clocking out parallel words from the register.

12. (Original) The receiver according to claim 11, wherein the receiver includes a bit alignment register to store received bit alignment words in order to locate the position of the bits in the serial to parallel register.

13. (Original) The receiver according to claim 12, wherein the receiver includes a CRC generator for generating a CRC code word in response to the received data, and a check circuit for checking a received CRC code word against the generated CRC code word.

14. (Canceled).

15. (Currently Amended) In an integrated circuit having a system clock, a transceiver comprising:

a receiver, including

a plurality of serial to parallel registers coupled to corresponding serial sub-links, for converting received serial data words from the sub-links into parallel form, and

a clock generator, responsive to the received data, for generating a low speed clock with a frequency nominally equal to the system clock; and

a transmitter as recited in ~~claim 1~~ claim 3 and adapted to be in communication with the receiver.